High Slew-Rate Amplifier Circuit For TFT-LCD System

BACKGROUND OF THE INVENTION

[0001] A liquid crystal display (referred to as an LCD hereinafter) is one of the most widely used flat panel displays at present. The LCD generally includes two substrates having a plurality of electrodes for generating electric field formed thereon, a liquid crystal layer interposed between the substrates and polarizers for polarizing light attached to outer surfaces of the respective substrates. The brightness of light from the LCD is controlled by applying voltages to the electrodes to rearrange liquid crystal molecules. A plurality of switching devices such as thin film transistors (referred to as TFTs hereinafter), connected to the electrodes, for switching the voltages applied to the electrodes are provided on one of the substrates.

[0002] The LCDs include driving units having source driving units and gate driving units and a controller for controlling the driving circuits to supply voltages for the electrodes through the switching devices. In general, the controller is provided external to the substrates, and the driving circuits are placed either within or external to the substrate.

[0003] Figure 1 is a block diagram of one configuration 1 of an output buffer for buffering applied voltages which are supplied to an LCD, according to the Background Art. In Fig. 1, the output buffer is implemented as N rail-to-rail (R2R) amplifiers 102 that each handle one bit of the N bit data being buffered in parallel by the output buffer. Though the R2R amplifier 102 implementation of Fig. 1 exhibits good output slew rates, it has problems that

include: sinking large amounts of current; and consuming large areas of the substrate upon source driving unit formed, i.e., a big footprint.

[0004] Figure 2 is a block diagram of another configuration of the output buffer, according to the Background Art, which attempts to improve upon the implementation of Fig. 1. In Fig. 2, rather than using N total R2R amplifiers 102 (as in Figure 1), the output buffer is implemented so as to include a plurality of amplifying circuits 202 and a controller 208. Each amplifying circuit 202 includes: a 1-bit op-amp using P-type transistors (P-type op amp) 204; and a 1-bit op-amp formed of N-type transistors (N-type op-amp) 206.

[0005] As is known, to better avoid degrading the liquid crystal material in the LCD, a signal provided by the output buffer should oscillate around a common voltage, V_{com}, e.g., $V_{com} = \frac{1}{2}V_{DD}$, rather than be substantially constant. The P-type op-amp 204 handles the positive polarity portion of such an oscillating signal and the N-type op-amp 206 handles the negative polarity portion of such an oscillating signal. The outputs of the op-amps 204 and 206 are connected together. The controller 208 controls the op-amps 204 and 206 to alternate as follows: when the P-type op-amp 204 is on, the N-type op-amp 206 is off; and vice-versa.

[0006] The controller 208 turns on/off the op-amps 204 and 206 in response to a control signal CTL-H and a control signal CTL-L. The controller 208 generates the controls signals CTL-H and CTL-L based upon a polarity signal, POL generated by a timing controller (not shown) that is indicative of the polarity of the data passing through the output buffer.

[0007] Figures 3A-3F are timing diagrams for the output buffer implementation of Fig. 2, according to the Background Art. Figure 3A is a waveform representing an output enable signal, e.g., which can be generated by the timing controller. Figure 3B is a waveform representing the polarity signal, POL. Figures 3C and 3D are waveforms of the CTL-H signal (see Figure 2) and the CTL-L signal (see Figure 2), respectively, from the controller 208. Figure 3E is a waveform (VH_PART; (see Figure 2)) representing the output of the P-type op-amp 204. And Fig. 3F is a waveform (VL_PART; (see Figure 2)) representing the output of the N-type op-amp 206.

[0008] Inspection of Figs. 3C and 3E reveals that the VH_PART waveform tracks the CTL-H signal. Similarly, inspection of Figs. 3D and 3F reveals that the VL_PART waveform tracks the CTL-L signal. But the tracking is not good: the VH_PART waveform (Fig. 3E) has a slow rising-time, as indicated by a reference number 302; and the VL_PART waveform (Fig. 3F) has a slow falling-time, as indicated by a reference number 304.

[0009] Slow rising/falling times produced by an output buffer are generally not desirable because, e.g., blurring of dynamic images on the LCD is proportional to slowness of rising/falling times. Thus, it is desirable to provide a high slew rate amplifying circuit for a TFT-LCD system.

SUMMARY

[0010] An embodiment of the invention provides a high slew rate amplifying circuit (e.g., for a TFT-LCD system). Such an amplifying circuit includes: an operational amplifier; a pull-up transistor connected to the output

of the operational amplifier; a pull-down transistor to the output of the operational amplifier; a control circuit to selectively actuate the pull-up transistor and the pull-down transistor, respectively.

[0011] According to an embodiment of the present invention, the control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/2 of the period of a polarity signal; or less than the period of a output enable signal. The control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/20 period of the polarity signal; or less than about 1/10 of the period of the output enable signal. The control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/200 of the period of the polarity signal; or less than about 1/100 of the period of the output enable signal.

[0012] According to an embodiment of the present invention, the control circuit includes: a first one-shot circuit to generate a first one-shot signal that determines actuation time of the pull-up transistor; and a second one-shot rising circuit to generate a second one-shot signal that determines actuation time of the pull-down transistor. The first and second one-shot signals are determined as a function of the output enable signal. Each of the first and second one-shot circuits includes at least one delay unit, respectively, to delay a transition in the respective one-shot signal relative to a transition in the output enable signal.

[0013] According to an embodiment of the present invention, the operational amplifier includes a high-part amplifying sub-circuit and a low-part amplifying sub-circuit. The high-part amplifying sub-circuit has voltage follower configuration including a plurality of transistors. The high-part amplifying sub-circuit further includes at least one capacitor. The low-part amplifying sub-circuit has voltage follower configuration including a plurality of transistors. The low-part amplifying sub-circuit further includes at least one capacitor.

[0014] According to an embodiment of the present invention, the pull-up transistor is connected to the output of the high-part amplifying sub-circuit and the pull-down transistor is connected to the output of the low-part amplifying sub-circuit.

[0015] A liquid crystal display (LCD) device is also provided, which includes: an LCD panel; and a plurality of source drivers connected to the panel; each of the source drivers including an output buffer.

[0016] Each output buffer includes: an operational amplifier; a pull-up transistor connected to the output of the operational amplifier; a pull-down transistor to the output of the operational amplifier; a control circuit to selectively actuate the pull-up transistor and the pull-down transistor, respectively.

[0017] Such an LCD device's control circuit is operable to selectively actuate each of the pull-up and pull-down transistors, respectively, for one of the following: less than about 1/2 of the period of a polarity signal; less than the period of an output enable signal; less than about 1/20 period of the

polarity signal; less than about 1/10 of the period of the output enable signal; less than about 1/200 of the period of the polarity signal; or less than about 1/100 of the period of the output enable signal.

[0018] Additional features and advantages of the invention will be more fully apparent from the following detailed description of example embodiments, the accompanying drawings and associated claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Figure 1 is a block diagram of one conventional configuration of an output buffer.

[0020] Figure 2 is a block diagram of another conventional configuration of an output buffer.

[0021] Figures 3A-3F are timing diagrams for the output buffer of Figure 2.

[0022] Figure 4 is a block diagram of an LCD system according to an embodiment of the present invention.

[0023] Figure 5 is a block diagram of a source driving unit according to an embodiment of the present invention.

[0024] Figure 6 is a block diagram of one configuration of the output buffer of Figure 1, according to an embodiment of the invention.

[0025] Figure 7 is a block diagram of the controller of Figure 6, according to an embodiment of the invention.

[0026] Figure 8A is a block diagram of the one-shot-high circuit of Figure 7, according to an embodiment of the invention.

[0027] Figure 8B is a block diagram of the one-shot-low circuit of Figure 7, according to an embodiment of the invention.

[0028] Figures 9A-9H are timing diagrams for the output buffer of Figure 6, according to an embodiment of the invention.

[0029] Figure 10A is a schematic partially depicting an example implementation of the high-part amplifier and pull-up transistor of Figure 6.

[0030] Figure 10B is a schematic partially depicting an example implementation of the low-part amplifier and pull-down transistor of Figure 6.

[0031] The accompanying drawings are: intended to depict example embodiments of the invention and should not be interpreted to limit the scope thereof; and not to be considered as drawn to scale unless explicitly noted.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0032] Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings. However, the embodiments of the present invention may be modified into various other forms, and the scope of the present invention must not be interpreted as being restricted to the embodiments. The embodiments are provided to more completely explain the present invention to those skilled in the art. The drawings are not to scale and so may exhibit exaggerations for clarity. Like numbers refer to like elements throughout.

[0033] An embodiment of the invention, in part, represents a recognition of the following. Adding one or more pull-up/pull-down transistors to the outputs of the P-type op-amp and the N-type op-amp can substantially improve

rise/decay times. But if the pull-up/down transistors are operated for a similar or substantially the same duration as the op-amps, they also substantially increase the amount of current being sunk by the output buffer. However, if one or more such pull-up/down transistors are operated for a shorter duration than the op-amps, then significant improvements in rise/decay times can be achieved without corresponding significant increases in the amount of current being sunk by the output buffer.

[0034] Figure 4 is a block diagram of an LCD system 400 according to an embodiment of the present invention. Referring to Figure 4, the LCD system 400 includes a TFT-LCD system 404 and a graphic controller 402 for providing display data to the TFT-LCD system 404. According to an embodiment of the present invention, the graphic controller 402 includes a signal-sending unit 406 which communicates the display data to a corresponding signal-receiving unit 416 in the TFT-LCD system 404. Many signaling techniques, e.g., low voltage differential signaling (LVDS), can be used by the signal sending and receiving units 406 and 416.

[0035] Referring to Figure 4, the TFT-LCD system 104 further includes: a timing controller 408 (of which the signal-receiving unit 416 is a part); gate driving units 412; source driving units 414; and a TFT-LCD panel 410. The timing controller 408 includes a signal-sending unit 418. After manipulating the display data received by the signal receiving unit 416, the timing controller 408 sends the manipulated data to the gate driving units 412 and the source driving units 414 via the signal-sending unit 118. The signal sending unit 418 can use the same signaling technique as the signal sending and receiving units

406 and 418, e.g., LVDS, or it can use other techniques, e.g., reduced swing differential signaling (RSDS) which is well known to those skilled in the art.

[0036] Figure 5 is a block diagram of one of the source driving units 414 of Figure 4. Each of the source driving units 414 includes: an N-bit shift register (SR) 502; data latches 504; a digital-to-analog converter (DAC) 506; and an output buffer 508. These units are generally cascade-connected such that data flows from the timing controller 408 to the TFT-LCD panel 410 through the following sequence of units: 502; 504; 506; and 508. The DAC 506 can be based primarily upon resistors, capacitors, or combination of resistors and capacitors.

[0037] Figure 6 is a block diagram of an output buffer 600 according to an embodiment of the present invention, e.g., for a TFT-LCD system. The output buffer 600 corresponds to the output buffer 508 of Figure 5.

[0038] The output buffer 600 of Figure 6 includes: a plurality of amplifying circuits 602; a first controller 608; and a second controller 616. Each amplifying circuit 602 includes: a first op-amp 604; a second op-amp 606; at least one pull-up transistor 612; and at least one pull-down transistor 610. According to an embodiment of the present invention, the first op-amp 604 can be an N-bit (wherein N is positive integer) op-amp made of P-type transistors and the second op-amp 606 can be an N-bit (wherein N is positive integer) op-amp made of N-type transistors. For example, each of the N-bit op-amps can be a one-bit op-amp having a voltage-follower configuration shown in Figures 10A and 10B. The pull-up transistor 612 is preferably made of the same impurity type, e.g., P-type, as the first op-amp 604 so as to be more

compatible. The pull-down transistor 610 is preferably made of the same impurity type, e.g., N-type, as the second op-amp 606 so as to be more compatible.

[0039] The first controller 608 of Figure 6 generates control signals CTL-H and CTL-L for the first op-amp 604 and the second op-amp 606, respectively. The first op-amp 604 handles the positive polarity portion of the oscillating input signal (received, e.g., from a DAC such as DAC 506) and the second op-amp 606 handles the negative polarity portion of the oscillating input signal (again, received, e.g., from a DAC such as DAC 506). Likewise, the outputs of the first and second op-amps 604 and 606 are connected together to provide the output of the buffer 600.

[0040] The first controller 608 controls (or actuates) the first and second op-amps 604 and 606 to alternate as follows: when the first op-amp 604 is on, the second op-amp 606 is off; and vice-versa. As such, the first controller 608 turns on/off (actuates) the first and second op-amps 604 and 606 as follows: the first op-amp 604 via the control signal CTL-H; and the second op-amp 606 via the control signal CTL-L. The control signals CTL-H and CTL-L are generated by the first controller 608 based upon the polarity signal, POL (which, again, is indicative of the polarity of the data passing through the output buffers 600 and can be generated by the timing controller 408 (in Figure 4).

[0041] In addition to being tied together, the outputs of the first and second op-amps 604 and 606 are: connected to the system source voltage, e.g.,

V_{DD}, via the pull-up transistor 612; and connected to the system ground voltage, e.g., V_{SS}, via the pull-down transistor 610.

[0042] The second controller 616 of Figure 6 controls the pull-up and pull-down transistors 612 and 610 via control signals HPU (Half Pull-up) and HPD (Half Pull-down), respectively. As will be discussed further below, the pull-up and pull-down transistors 612 and 610 are operated for a shorter duration than the first and second op-amps 604 and 606, which achieves significant improvements in the rising/falling times without corresponding significant increases in the amount of current being sunk by the output buffer 600. The pull-up transistor 612 and the pull-down transistor 610 are operated via the control signals HPU and HPD, respectively, generated by the second controller 616.

[0043] Figure 7 is a block diagram of the second controller 616 of Fig. 6, according to an embodiment of the present invention.

[0044] The second controller 616 of Figure 6 includes a one-shot-high circuit 702 and a one-shot-low circuit 704, which generate the control signals HPD and HPU, respectively, based upon the output enable signal OE (which, again, can be generated by the timing controller 408 of Fig. 4).

[0045] Figure 8A is a block diagram of the one-shot-high circuit 702 of Fig. 7, according to an embodiment of the present invention. The circuit 702 includes: a plurality of non-inverting (or buffering) op-amps 802 (here, for example, a total of four); an inverter 804; and an OR gate 806. The buffering op-amps 802 are cascade-connected between the output enable signal and the inverter 804. The output of the inverter 804 is connected to one of the inputs

to the OR gate 806. The other input to the OR gate 806 directly receives the output enable signal OE. In operation, the one-shot-high circuit 702 delays the start of operation of the pull-up transistor 612 (in Figure 6) relative to a start time of the first op-amp 604, and then operates the pull-up transistor 612 (in Figure 6) for a relatively shorter duration than the P-type op-amp 604.

[0046] Figure 8B is a block diagram of the one-shot-low circuit 704 of Fig. 7, according to an embodiment of the present invention. The circuit 704 includes: a plurality of non-inverting (or buffering) op-amps 808 (here, for example, a total of four); an inverter 810; and an AND gate 812. The buffering op-amps 808 are cascade-connected between the output enable signal OE and the inverter 810. The output of the inverter 810 is connected to one of the inputs to the AND gate 812. The other input to the AND gate 812 directly receives the output enable signal. In operation, the one-shot-low circuit 704 delays the start of operation of the pull-down transistor 610 relative to a start time of the second op-amp 606, and then operates the pull-down transistor 610 for a relatively shorter duration than the second op-amp 606.

[0047] A specific numerical example of operation times/durations of the pull-up and pull-down transistors 612 and 610 will be provided. Assume that the period of the polarity signal, POL, is about 80 μ-sec. Recall that the first op-amp 604 is operated during the positive polarity portion thereof while the second op-amp 606 is operated during the negative polarity portion. As such, each of the op-amps 604 and 606 is turned on for about 40 μ-sec. Each of the pull-up transistor 612 and the pull-down transistor 610 can be turned on about 0.5 μ-sec after the polarity signal POL transitions from positive polarity

to negative and vice-versa; this can be referred to as the delay time. And each of the pull-up transistor 612 and the pull-down transistor 610 can be kept on for a duration of about 0.1 μ-sec, after which each can be switched off until the next transition in the polarity signal POL.

[0048] The ordinarily-skilled artisan will understand that the delay time and the duration can, and should, vary according to the circumstances to which the output buffer 600 is applied. The choice of the duration can be viewed from the perspective of the economic maxim: diminishing returns. As the duration is increased, the improvement in slew rate becomes progressively more offset (in terms of advantages/disadvantages) by the increases in current sunk by the output buffer 600.

[0049] The pull-up and pull-down transistors 612 and 610 can be activated for a duration, respectively, that is: less than about 1/20 period of the polarity signal POL, or less than about 1/10 of the period of the output enable signal OE; or alternatively less than about 1/200 of the period of the polarity signal POL, or less than about 1/100 of the period of the output enable signal.

[0050] Figures 9A-9H are timing diagrams for the output buffer of 600 of Fig. 6, according to an embodiment of the present invention. Figure 9A is a waveform representing an output enable signal OE, e.g., which can be generated by the timing controller 408 (in Figure 4). Figure 9B is a waveform represent the polarity signal, POL. Figures 9C and 9D are waveforms representing the CTL-H signal and the CTL-L signal, respectively, from the controller 608 (in Figure 6). Figure 9E is a waveform representing the control

signal HPU. Figure 9F is a waveform representing the control signal HPD. Figure 9G is a waveform (VH_PART) representing the output of the first op-amp 604 (as pulled up by the pull-up transistor 612 according to the control signal HPU). And Fig. 9H is a waveform (VL_PART) representing the output of the second op-amp 406 (as pulled down by the pull-down transistor 610 according to the control signal HPD).

[0051] Inspection of Figures 9C and 9G reveals that the VH_PART waveform tracks the CTL-H signal. Similarly, inspection of Figures 9D and 9H reveals that the VL_PART waveform tracks the CTL-L signal. In contrast to the Background Art, however, the tracking is better. The VH_PART waveform (Fig. 9G) has a high/fast rising-time, as indicated by reference number 902; and the VL_PART waveform (Fig. 9H) has a high/fast falling-rate, as indicated by reference number 904. Taking the view that an LCD panel 410 (in Figure 4) is a large resistive-capacitive load, the high slew rate of the output buffer 600 indicates that the output buffer 600 correspondingly charges/discharges the resistive-capacitive load faster as contrasted with the output buffer of Background Art Fig. 2.

[0052] Figure 10A is a schematic partially depicting an example implementation of the first op-amp 604 and the pull-up transistor 612 of Fig. 6. Similarly, Fig. 10B is a schematic partially depicting an example implementation of the second op-amp 606 and the pull-down transistor 610 of Fig. 6.

[0053] In Figure 10A, the first op-amp 604 has voltage follower configuration which includes a plurality of transistors 1002-1016. The first op-

amp 604 further can include at least one capacitor 1018. As the voltage follower configuration is well known to those skilled in the art, detailed description is omitted. Operationally in Figure 10A, an INPUT signal at an input port is transformed to an OUTPUT signal (available at an output port) in response to the control signal HPU.

[0054] In Figure 10B, the second op-amp 606 has voltage follower configuration which includes a plurality of transistors 1022-1036. The second op-amp 606 further can include at least one capacitor 1038. As the voltage follower configuration is well known to those skilled in the art, detailed description is omitted. Operationally in Figure 10B, an INPUT signal at an input port is transformed to an OUTPUT signal (available at an output port) in response to the control signal HPD.

[0055] The invention may be embodied in other forms without departing from its spirit and essential characteristics. The described embodiments are to be considered only non-limiting examples of the invention. The scope of the invention is to be measured by associated claims. All changes which come within the meaning and equivalency of the claims are to be embraced within their scope.